IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application
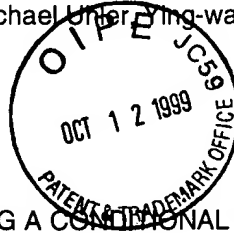
Inventor(s): Radhika Thekkath, Michael Uhler, Ying-wai Ho, and Chandlee Harrell

Group Art Unit:

Filed: 07/30/99

Examiner:

Serial No.: 09/364/789

Title: PROCESSOR HAVING A CONDITIONAL BRANCH EXTENSION OF AN INSTRUCTION SET ARCHITECTURE

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
DJC	A	5,671,401	09/23/97	Harrell	395	505	05/08/95
DJC	B	5,793,661	08/11/98	Dulong et al.	364	750.5	12/26/95

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	No
	C							
	D							
	E							
	F							
	G							
	H							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
DJC	I	Higakl et al.; A 2.5 GFLOPS 6.5 MILLION POLYGONS PER SECOND 4-WAY VLIW GEOMETRY PROCESSOR WITH SIMD INSTRUCTIONS AND A SOFTWARE BYPASS MECHANISM; Nakahara-ku, Kawasaki, Japan
DJC	J	Advanced Micro Devices, Inc.; 3D NOW! TECHNOLOGY MANUAL; 1998
DJC	K	Motorola Inc.; ALTIVEC TECHNOLOGY PROGRAMMING ENVIRONMENTS MANUAL; 05/1998

Examiner	Daniel J Chang	Date Considered	6/26/02

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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APPLICANT
Thekkath et al.

FILING DATE
July 30, 1999

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS
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	AB1	4,879,676	11/1989	Hansen	364	748
	AC1	5,185,713	02/1993	Kobunaya	364	748
	AD1	5,392,228	02/1995	Burgess et al.	364	715.04
	AE1	5,517,438	05/1996	Dao-Trong et al.	364	748
	AF1	5,550,768	08/1996	Ogilvie et al.	364	748
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	AH1	5,726,927	03/1998	Wolrich et al.	364	754
	AI1	5,729,724	03/1998	Sharangpani et al.	395	563
	AJ1	5,774,709	06/1998	Worrell	395	580
	AK1	5,790,827	08/1998	Leung	395	392

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
							Yes No
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

D7L	AR	1	Heinrich, Joe, *MIPS R4000 Microprocessor User's Manual*, Second Edition, MIPS Technologies, 1994, pp. 154-155, 157, 159, 161, 168, 170-171, B-9, B-10, B-13, B-17, B-19, B-21, B-23, B-27, B-38, B-40 and B-62 (19 pages total). Note: The page count of this document was cited to us as listed here in an International Search Report from a MIPS PCT application.
D7L	AS	1	*AltiVec™ Technology Programming Environments Manual*, Preliminary REV 0.2, May 1998, pp. 4-16 thru 4-19 (4 pages total).
D7L	AT	1	American National Standards Institute, An American National Standard - *IEEE Standard for Binary Floating-Point Arithmetic*, (IEEE Std 754-1985), New York, New York, ©1985, pp. I-vi and 1-14.

DATE CONSIDERED 6/06/02

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
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	AJ2	6,065,115	05/2000	Sharangpani et al.	712	235	
DJC	AK2						

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

DJC	AR	2	3DNow!™ Technology Manual, Advanced Micro Devices, 1998, pp. I-x and 1-62 (72 pages total).
DJC	AS	2	TMS32010 User's Guide, Texas Instruments, 1983, p. 1183.
DJC	AT	2	Copy of International Search Report for PCT Application Number PCT/US00/03900, 6 pages, Mailed July 20, 2000.

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